

ABSTRACT

We will presents the design and FPGA implementation of sequential digital 8-tap FIR filter using a novel micro programmed controller based design approach. In the paper, the FIR filter is designed for operation controls by micro programmed controller. The proposed FIR filter will be coded in VHDL using modular design approach, and implement in Spartan-3E FPGA. The performance evaluation and synthesis results obtained through Xilinx ISE synthesis tool and functionally checked in Model sim module.

KEYWORDS: FIR filter, Implementation of FIR filter, Micro programmed controller

INTRODUCTION

Filters are a basic component of all signal processing and telecommunication systems. Filters are widely adopted in many areas like signal processing and communication systems, applications such as noise reduction, channel equalization, audio processing, radar, biomedical signal processing, video processing, and analysis of financial data and economic. For example in a radio receiver tuners or band-pass filters are used to extract the signals from a radio channel. In an audio graphic equalizer the input signal is filtered into a number of sub-band signals and the gain for each sub-band can be varied manually with a set of controls to change the perceived audio sensation. In a Dolby system pre-filtering and post-filtering are used to minimize the effect of noise. In wireless audio a compensating filter may be included in the preamplifier to compensate for the non-ideal frequency-response characteristics of the speakers.

Filters are also used to create effective audio-visual effects for films, music and in broadcast studios.

The primary functions of a filter are one or more of the followings:

- To confine a signal into a prescribed frequency band or channel
- To decompose a signal into one than more sub-band signals for sub-band signal processing
- To modify the frequency spectrum of a digital signal.
- To model the input-output relation of a system such as a mobile communication channel, voice production, musical instruments, room acoustics and telephone line echo.

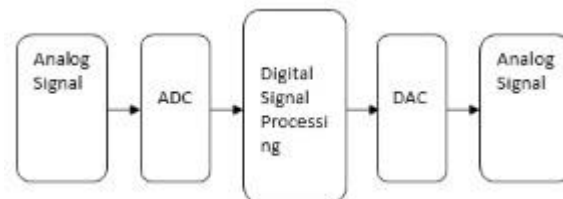


Figure 1.1 block diagram of DSP

Digital finite impulse response (FIR) filters are the basic building block of many digital signal processing (DSP) systems. FIR Filters are used due to their stability and linear phase properties. The main works of digital FIR filters are to filter out undesirable parts of the signal shape the spectrum of signals in communication channels, signal detection or analysis in radar applications. Adders, multipliers and delay elements are the main components used in the implementation of digital FIR filters. These components are arranged and interconnected in different ways based on the architecture of the FIR filter.

FIR filter performs a convolution on a window of N data samples which can be mathematically expressed as follows:

$$y(n) = \sum_{k=0}^{N-1} h(k) \cdot x(n-k)$$

PROPOSED METHOD FOR FIR FILTER

Fir filter is implemented using shift and add method. We perform all out optimization in the multiplier block. The constant multiplications are decomposed in to additions and shifts and the multiplication complexity is reduced. It's possible to implement the design in the two form described below.

- The coefficients are changed to integer getting multiplied to a multiple power of 10, and then we arrange these coefficients positive power of n.
- First arrange decimal coefficients according to negative and positive power of 2 (no need to them into integer). So the filter hardware and power consumption will reduce.

COMPARISON BETWEEN ANALOG FILTER AND DIGITAL FILTER

The principal advantage of digital filters is the flexibility available in their design. You can design almost any band shape you want with a digital filter, especially those with very steep cut-off slopes that are very difficult to achieve with ordinary components. Digital filters provide guaranteed stability. In addition, they provide linear phase-frequency characteristics that most analog filters cannot have, especially when narrow bands or steep cut-offs are required.

FIR filter

A FIR-filter (Finite input response filter) is a digital filter that is widely used in digital signal processing applications. The FIR-filter calculates an output from setoff input-samples. The set of N input samples is multiplied by a set of coefficients and then added together to produce the output $y(n)$ see Fig. 4.1. The filter behavior is determined by the filter-coefficients. A general FIR filter is described in the following equation:

$$Y(n) = k_1x(n) + k_2x(n-1) + k_3x(n-2) \dots k_mx(n-m)$$

Where k_i is the coefficient i . x is the input signal and y is the output signal. m is the number of filter coefficients $\frac{3}{4}$ called taps, and n is the input sample number.

Implementation of FIR-filters can be undertaken in either software or hardware. A software implementation will require sequential execution of the filter-functions. Hardware design of FIR-filters allows the filter functions to be executed in a parallel manner which make sim proved filter processing speed possible.

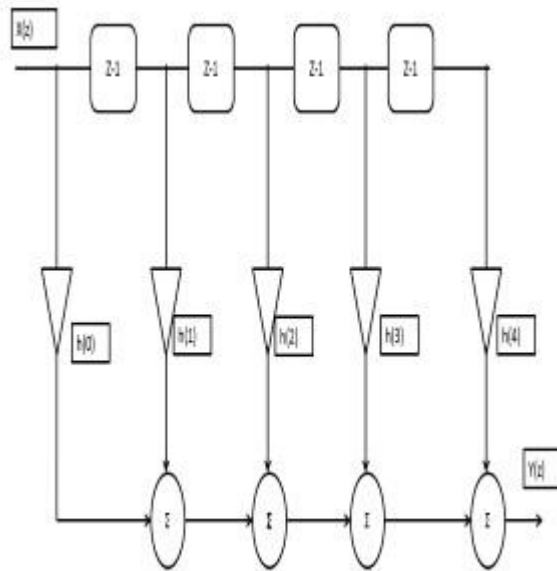


Figure: 4.1 FIR filter

IMPLEMENTATION OF FIR FILTER

In this paper, MAC architecture is considered. There is a design and implementation of low power multiplexer based shift/add multiplier for reduction of power consumption. FIR filter are implemented using the shift and add method. We perform our optimization in the multiplier block. This multiplier constituted of one shifter block (barrel shifter) one adder block and also control unit, where as shifter block is based on multiplexer only. And proportional to select signal (shift[2..0]) input number left shift to magnitude 0 to 7 magnitude of shift specification by control unit i.e. based on weight of bits input signal to control unit. If slightly bit is zero we have non-shift

and slightly bit is one to magnitude weight of bit shift is apply. That is continuing show VHDL code of this block. And will have been explanation in related with shifter blocks. Adder blocks add together shifted number, final product favorable output. By implementation of shifter block based on multiplexer hardware and power consumption of FIR filter is much reduced. In Fig. 5.1 shown block diagram of low power multiplexer based shift/add multiplier. The constant multiplications are decomposed in to additions and shifts and the multiplication complexity is reduced. It's possible to implement the design in the two forms described below:

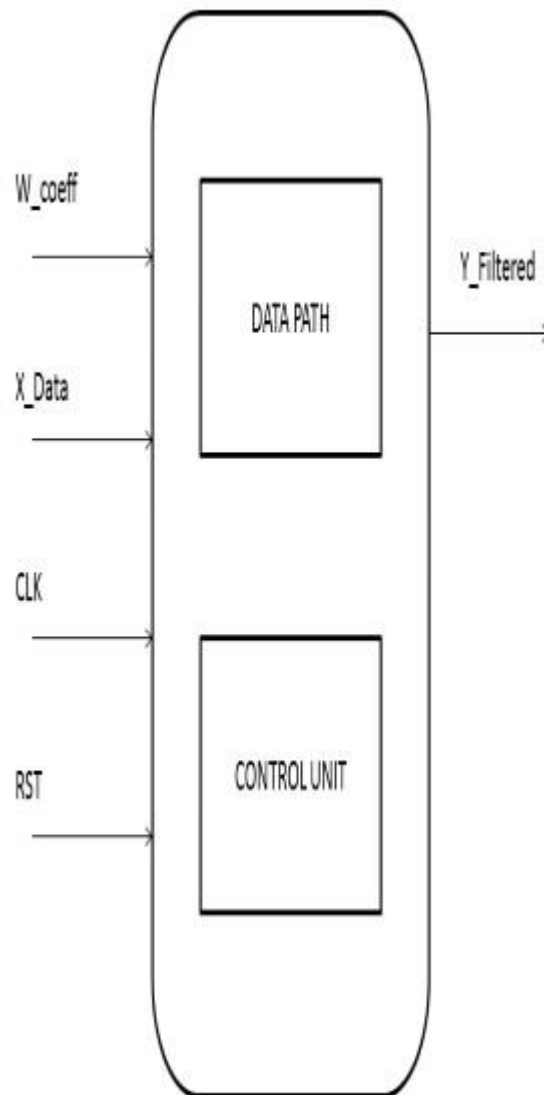


Figure 5.1 illustrates the data path architecture of FIR filter.

MICROPROGRAMMED CONTROLLER

There are numerous methods to design the controller, such as hardwired controller and micro programmed controller. In this paper, we used micro programmed controller to systematize the operation of FIR filter. The leading advantage of the micro programmed controller is its flexibility to append or alter by simply changing the micro program in the ROM based control

memory. This makes the design of larger tap FIR filter much simpler. The tap coefficients (w_0, w_1, w_2, w_3) are loaded with data based on load enable (LE) signal. Once loading the input data in the first register, the input data is multiplied and accumulated based on the select signals (S1 and S0), product select (Ps) and load accumulator (lacc) signals.

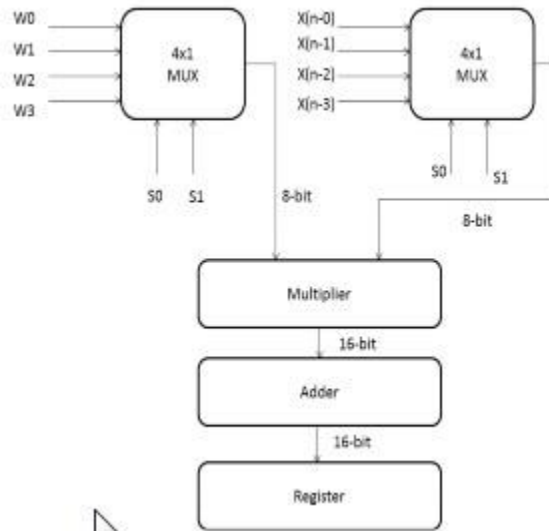


Figure 6.1 Architecture of FIR filter

OBSERVATION AND RESULT

R. RajaSulochana, Vasuja devi Midasala, S Naga kishore Bhavanam, Jeevan Reddy K [2]-

This paper presents the methods to reduce dynamic power consumption of a digital Finite Impulse Response (FIR) filter these methods include low power serial multiplier and serial adder, combinational booth multiplier, shifter adder and multipliers, They have implemented their paper using XILINX ISE and hardware used is Spartan-3E and family is XC2S200E.

RUPALI MADHUKAR NARSALE and DHANASHRI GAWALI [4] –

This paper reviews presents the methods to reduce dynamic power consumption of a digital Finite Impulse Response (FIR) filter. To reduce power consumption they reviewed some techniques such as Modified Booth Encoding Algorithm combined with Spurious Power Suppression Technique, Low Power Digit Serial Multiplier along with carry look ahead adder, shift/add multipliers etc and reduce dynamic power up to 95%.

A.Renuka Narasimha, K.Rajasekhar, A.Sujana Rani[6]-

In This paper they have presented a low power and low area FIR filter, for reduce power consumption and area they used Modified Booth Encoding Algorithm combined with Spurious Power Suppression Technique, folding transformation in linear phase architecture of digital filter, Low Power Digit Serial Multiplier along with carry look ahead adder, shift/add multipliers. The proposed FIR filters reduce number of slices by 12%.

Tejinder Singh and Balwinder Singh Dhaliwal [7]

– In their paper they have focus on efficient implementation of FIR filters, for that they have used a Booth Radix-8 multiplier. For implementation of the said FIR filter MATLAB FDA Tool is employed to determine various filter coefficients. The 8th order FIR filters have been designed using VHDL language. FPGAs implementation results show that the proposed design filter has an improved speed in comparison to previous published results.

Table 1

No	Method	Number of Slices
11	FIR filter based shift add multiplier	8 out of 9312 (0.86mw)
32	Using a low power MAC unit with clock gating and pipelining	Dynamic power consumption of digital filter by pipelining up to 95%.

13	Booth multiplier	585 out of 4656 12%
44	MAC booth	19 (100mw)

APPLICATION

- Digital FM stereo

A digital FM stereo decoder uses the phase characteristics of linear phase FIR filters, together with a mathematical operation, to generate a 38 kHz subcarrier signal from a 19 kHz pilot. The subcarrier signal is mixed with the input composite signal from which the pilot has been removed to shift its L-R component to baseband; the linear phase FIR filters also maintain phase coherence between the subcarrier and the composite signals.

- SONAR

Different digital filters used in sonar signal processors perform two major functions, the filtering of waveforms to modify the frequency content and the smoothing of waveforms to reduce the effects of noise.

- RADAR

Digital processing has also permitted increased capability for extracting target information from the radar signal. SAR provides an image of a scene. Radars are used to recognize one type of target from another, with the help of digital processing,

DRAWBACK

The main disadvantage of digital filters is that the signals must be sampled and converted to digital form. This always entails loss of resolution (accuracy), bandwidth limitations, and introduces noise. These effects can be minimized by high sample rates and depth (no of bits per sample) and filter size (no of samples) but those come with more components, large processing speed required.

FUTURE SCOPE

The present work on the new multiplier architecture can be further extended in various directions. The design can be simulated to check the power consumption. Other methods can be implementing with this to further improve the delay. In order to carry out complete analyze, the circuit can be extended to chip level where the delays due to wiring, PAD and interconnects are included.

CONCLUSION

From the above observation table we can concluded that Filter based shift and add multiplier we can design less power consuming circuit as compare to other method listed in above method.

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